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A Simulation Methodology for Single-Electron Multiple-Valued Logics and Its Application to a Latched Parallel Counter

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SUMMARY This paper introduces a methodology for simulating single-electron-transistor (SET)-based multiple-valued logics (MVLs). First, a physics-based analytical model for SET is described, and then a procedure for extracting parameters from measured characteristics is explained. After that, simulated and experimental results for basic MVL circuits are compared. As an advanced example of SET-based logics, a latched parallel counter, which is one of the most important components in arithmetic circuits, is newly designed and analyzed by a simulation. It is found that a SET-based 7-3 counter can be constructed with less than 1/10 the number of devices needed for a conventional circuit and can operate at a moderate speed with 1/100 the conventional power consumption.

key words: *single-electron transistor (SET), multiple-valued logic (MVL), counter, analytical model, SPICE*

1. Introduction

Single-electron transistors (SETs) [1], [2] are very attractive for future nanoelectronics applications because they are expected to operate in less space with less power consumption. Moreover, SETs are suitable for multiple-valued logic (MVL) due to the discrete number of electrons in a Coulomb island, which can be directly related to the multiple signal levels for MVL [3], [4]. The discreteness of the electronic charge in the island results in periodic transfer characteristics, which are also useful when counting or decoding multiple signal levels [5].

However, studies of SET-based MVLs have just started [3], [4], and a design and simulation methodology is not yet well established. In this paper, we will briefly summarize the model [6] for simulating circuits with SETs, and then explain the procedure for extracting parameters from experimental data. We then compare simulation results for basic MVL components with previously obtained experimental results [4], [7]. As an advanced example of SET-based logics, a latched parallel counter is newly designed and analyzed by using a simulation.

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2. Simulation Model

Figure 1(a) shows the equivalent circuit of a SET, which consists of two tunnel junctions and a Coulomb island whose electrical potential is controlled by a gate and a backgate. Although not essential, the backgate is sometimes useful for adjusting the "phase" of the I_d-V_{gs} oscillation. Because of the high charging energy resulting from the small total capacitance C_Σ around the island, spontaneous tunneling at junctions is prohibited (Coulomb blockade) and the number of electrons in the island becomes discrete under the control of the gates. The drain current changes periodically with respect to the gate voltages, and exhibits valleys and peaks, respectively, at integer and half-integer numbers of electrons in the island (Fig. 1(b)).

In the proposed single-electron multiple-valued logic [4], SETs are combined with MOSFETs and other passive components such as capacitors. Therefore, we developed a new analytical SET model [6] and implemented it in a standard circuit simulator SPICE [8].

In the SET model, the Coulomb island and the source/drain leads are assumed to be metallic, and the source/drain tunneling resistances R_s/R_d may be asymmetric, as long as they are larger than the resistance quantum, h/e^2, of about 25.8 kΩ. The capacitance parameters may have arbitrary values.

For the SET to be regarded as an independent circuit element and for the transient analysis to be performed without considering the capacitance model, every terminal should be driven by a constant-voltage (CV) source or connected to a large capacitor whose value is much larger than the total ca-

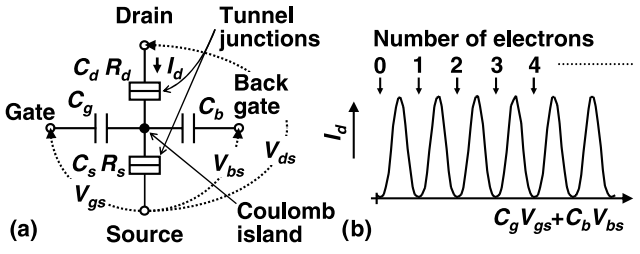

Fig. 1 Equivalent circuit (a) and transfer characteristics (b) of a SET. The number of electrons in the Coulomb island is controlled by the gate and the backgate via gate capacitor C_g and backgate capacitor C_b, respectively. Drain current I_d flows periodically with respect to gate voltages V_{gs}, V_{bs}, where the number of electrons is half-integer.

pacitance C_Σ (= $C_g + C_b + C_s + C_d$) of the SET.

The model is based on the steady-state master equation, and takes only the two most-probable charging states into account. The drain current I_n, corresponding to the numbers of electrons n and $n+1$ in the Coulomb island, can be simply expressed by using the newly introduced asymmetry factor $r = (R_d - R_s)/(R_d + R_s)$ and the hyperbolic sine functions [6].

$$I_n = \frac{e}{4C_\Sigma R_T} \frac{(1-r^2)(\tilde{V}_{gs}^2 - \tilde{V}_{ds}^2)\sinh(\tilde{V}_{ds}/\tilde{T})}{A} \quad (1)$$

$$A = \{\tilde{V}_{gs}\sinh(\tilde{V}_{gs}/\tilde{T}) - \tilde{V}_{ds}\sinh(\tilde{V}_{ds}/\tilde{T})\} + r\{\tilde{V}_{ds}\sinh(\tilde{V}_{gs}/\tilde{T}) - \tilde{V}_{gs}\sinh(\tilde{V}_{ds}/\tilde{T})\} \quad (2)$$

$$\tilde{V}_{gs} = \frac{2C_gV_{gs}}{e} + \frac{2C_bV_{bs}}{e} - \frac{(C_g + C_b + C_s - C_d)V_{ds}}{e} - 2n - 1 \quad (3)$$

where $\tilde{V}_{ds}$ is the normalized drain-to-source voltage, $C_\Sigma V_{ds}/e$, $\tilde{T}$ the normalized temperature, $k_BT/(e^2/2C_\Sigma)$, and R_T the harmonic mean of the tunneling resistances, $2R_dR_s/(R_d + R_s)$. A summation of I_n's for different n's in the relevant gate-voltage range causes the drain current to oscillate periodically and simultaneously compensates for the inaccuracy caused by the insufficient number of charging states considered in the model.

Comparison with a Monte Carlo simulation revealed that the error in the modeled drain current is less than 5% when $\tilde{V}_{ds}$ and $\tilde{T}$ are less than 1 and 0.1, respectively, although the model is very simple [6].

The SET model was implemented in SmartSpice [8] as a subcircuit comprising analog behavioral devices. The main part of the code consists of only 20 lines, but the model is accurate and can be used both for DC and transient analyses as long as each terminal is connected to a CV source or a capacitor larger than C_Σ.

3. Parameter Extraction

The parameters for the SET model were extracted from experimental data for a device fabricated by the pattern-dependent oxidation (PADOX) process [9], [10]. As shown in Fig. 2, the positive slope, negative slope, and period of the Coulomb diamond plot (drain conductance contour plot in the V_{ds}-V_{gs} plane) correspond to $C_g/(C_s+C_g+C_b)$, $-C_g/C_d$ and e/C_g, respectively. Consequently, capacitance parameters, $C_s + C_b$, C_d and C_g can be obtained from the plot. We can obtain C_b when we consider that the current oscillation period in the I_d-V_{bs} characteristics is e/C_b or that the shift of the I_d-V_{gs} curve caused by the application of V_{bs} is formulated as $\Delta V_{gs}/\Delta V_{bs} = -C_b/C_g$. In this particular case, C_b is negligible, and C_g, C_d and C_s are calculated to be 0.27, 2.7 and 2.7 aF, respectively. For a symmetric case ($R_d = R_s$ and therefore $r = 0$), it can be seen from (1)–(3) that the drain current I_n reaches its maximum value, $V_{ds}/4R_T$, at $\tilde{V}_{gs} = 0$. Thus, the R_T (= $R_d = R_s$) can be calculated from the peak drain current in the I_d-V_{gs} or I_d-V_{bs} characteristics.

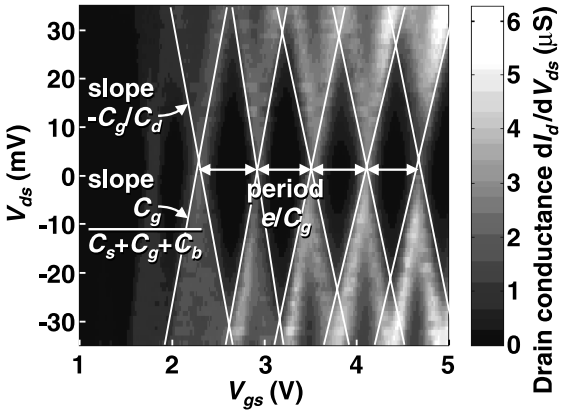

Fig. 2 A Coulomb diamond (drain conductance contour) plot of a SET fabricated by the PADOX process, measured at 27K [4]. Capacitance parameters, C_g, C_b, C_s and C_d, are extracted from the slopes and the period.

In an asymmetric case, the R_T obtained by the above procedure can be used as an initial value for an optimization that minimizes the difference between the model and experimental characteristics by varying R_d and R_s. We obtained $R_d = R_s = 120\,\mathrm{k\Omega}$ for the PADOX device shown in Fig. 2.

4. Comparison with Experiment

Figure 3 shows the measured I_d-V_{gs} characteristics of the SET in Fig. 2 together with a curve simulated using the analytical SET model. Periodic drain-current peaks are reproduced clearly by the simulation. As often observed in semiconductor SETs, the peak heights are uneven and the positions are not perfectly periodic, whereas the simulation, which assumes metallic leads and a metallic island, provides regular characteristics. But the degree of irregularity in the experimental data is acceptable for the demonstrations of 6-valued operation described below. We assumed a temperature of 17K to compensate for the difference between the electronic states in the semiconductor and metal. The maximum voltage gain C_g/C_d (inverting) and applicable voltage e/C_Σ for this SET are only 0.1 and 28 mV, respectively. However, this disadvantage will be covered by using a MOSFET in the proposed MVL.

Figure 4 shows the subthreshold characteristics of a MOSFET fabricated on the same SOI wafer for drain voltages of 5 V and 10 mV. The gate length and width and the gate oxide thickness are 14 μm, 12 μm, and 90 nm, respectively. This MOSFET will be connected to the SET drain in a cascode manner to compensate for the small voltage gain and the small applicable voltage of the SET. To maintain the constant drain voltage of the SET, the subthreshold slope of the MOSFET should be steep and the threshold voltage (V_{th}) shift due to the drain voltage should be small. We used the BSIM3 model [11] for the simulation, although the parameter optimization was preliminary.

Before discussing the results for more complex circuits including SETs and other components like MOSFETs and capacitors, it should be stressed that all the SET terminals

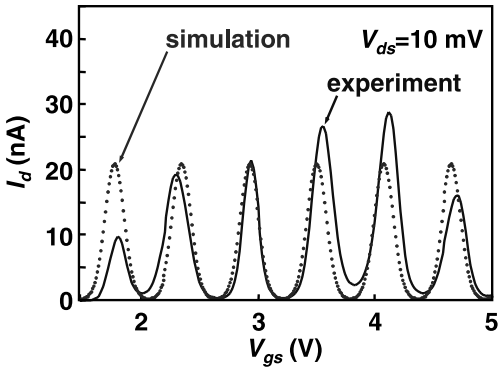

Fig. 3 I_d-V_{gs} characteristics of the fabricated SET, measured at 27K (solid line) [4]. Simulated characteristics with the analytical SET model are also shown (dotted line).

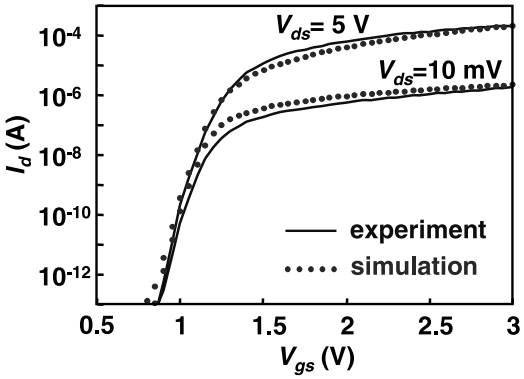

Fig. 4 I_d-V_{gs} characteristics of a MOSFET fabricated on the same SOI wafer as the SET, measured at 27K (solid line) [4]. Characteristics simulated by the BSIM3 model [11] are also shown (dotted line). The channel width and length and gate oxide thickness are 12 μm, 14 μm, and 90 nm, respectively. The measured threshold voltage V_{th}, corresponding to I_d = 4.5 nA and V_{ds} = 3 V, is 1.07 V.

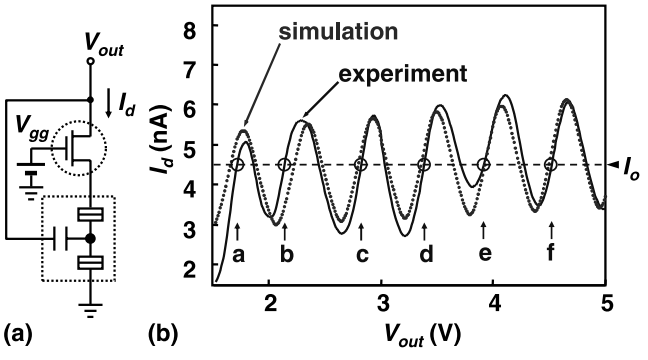

Fig. 5 Schematic diagram (a) and I_d-V_{out} characteristics (b) of the two-terminal multipeak NDR device. The experimental data (solid line) [7] were obtained at a V_{gg} of 1.08 V. Simulated characteristics obtained by SPICE are also shown (dotted curve). Stability points (a~f) expected for a current load of 4.5 nA are indicated by circles.

are connected to a CV source or a capacitor whose value is much larger than C_Σ. This condition is almost automatically satisfied with capacitances included in the MOSFET or wiring capacitances, because C_Σ is as small as 5.7 aF.

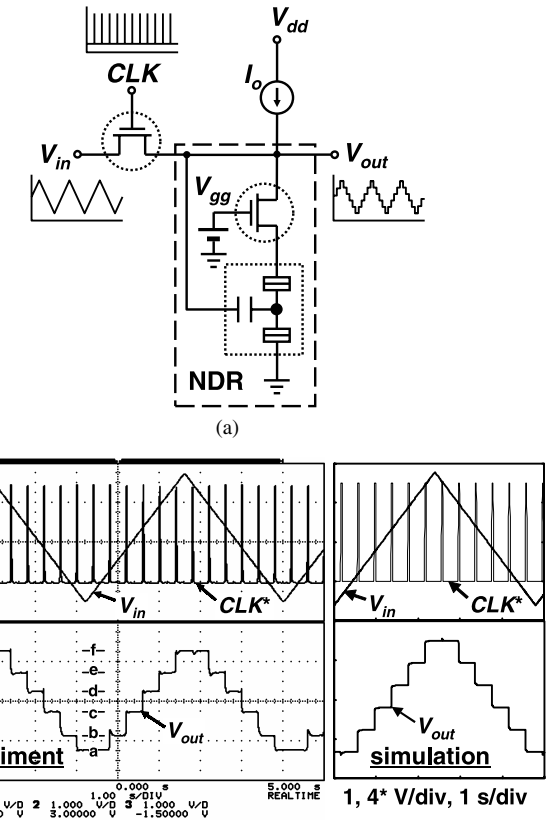

Fig. 6 Schematic diagram (a) and experimental [4] and simulated waveforms (b) of the quantizer.

The simulation reproduces the characteristics of the multipeak negative-differential resistance (NDR) device shown in Fig. 5(a). In this circuit, the periodic input/output characteristics of a SET are converted to two-terminal characteristics by shorting the MOSFET drain and SET gate. Figure 5(b) shows the two-terminal I_d-V_{out} characteristics of the multipeak NDR device. The current increases and decreases periodically, reflecting the I_d-V_{gs} characteristics of the discrete SET. If we were to connect a constant-current (CC) load of 4.5 nA, stability points a~f would appear. These multistate characteristics are very useful in constructing a quantizer or a multiple-valued memory. The peak-to-valley current ratio (PVCR) of the NDR device shown is 2.1 at most and much smaller than that of the discrete SET in Fig. 3. This is because the MOSFET is not an ideal constant voltage source for the SET drain in that an increase in the drain voltage increases the valley current and a reduction in the drain voltage reduces the peak current.

We also performed a transient simulation of the latched quantizer shown in Fig. 6(a). A triangular wave was fed to V_{in}, and the transfer-gate MOSFET was driven by short CLK pulses. Different voltage levels in the triangular wave were sampled by the MOSFET, transferred to the storage node, V_{out}, and quantized. V_{out} remains constant (latched) as long as the transfer-gate MOSFET is off. The waveforms are shown in Fig. 6(b). V_{out} was quantized to levels a~f,

which correspond to the stability points in Fig. 5. The simulation reproduces the experiment very well. The operating speed in the figure is limited by the large stray capacitance of 370 pF† at V_{out}.

5. Latched Parallel Counter Design

A counter is one of the most important components in arithmetic circuits, since most adders, including redundant-number adders, can be represented as generalized counters in the framework of counter tree diagrams (CTDs) [12]. In the simple case of a binary N-M parallel counter, the number of 1s in the input signals is counted as follows. The N binary signals are added to an $(N+1)$-valued signal ranging from 0 to N, and then the $(N+1)$-valued signal is decomposed into M binary signals as in the case of analog-to-digital converters. The truth table of a 3-2 counter is shown in Table 1 as an example. The number of '1' inputs, which is a 4-valued signal between 0 and 3, is converted to 2-digit binary-coded data. Note that the 3-2 counter is actually a full adder, if we consider i_2 and o_1 as the carry input and output, respectively.

Figure 7 shows the SET-based implementation of a 7-3 counter, which consists of an inverting adder, a latched quantizer, a voltage divider, and periodic literals with a negative output [5]. The quantizing function, i.e. level-restoring function, is essential because the analog adder always includes an intolerable error when it accumulates in multistage circuits. The latching function is also useful in multistage synchronous circuits. In this implementation, the periodic transfer characteristics of the SET are effectively utilized in the quantizer and literals. Each SET is combined with a MOSFET to keep the SET drain voltage nearly constant at a low voltage so that the Coulomb blockade condition is sustained, and to enhance the voltage gain. MOSFETs M2 and M3 are also used to select the function of addition or quantization with complementary clocks ϕ and ϕn. Specifically, the inverting adder is activated when ϕn is high, and the data are quantized and latched when ϕ is high. For literals, MOSFETs M4-6 are p-channel and the supply voltage V_{ddn} is set at a negative value to output negative voltages. This is consistent with the negative input voltages for the inverting adder. Note that the same SET can operate under both positive and negative drain voltages, and there is only one kind of SET in this counter.

Table 1 Truth table of a 3-2 counter.

input $i_2\ i_1\ i_0$	# of '1' inputs	output $o_1\ o_0$
0 0 0	0	0 0
0 0 1	1	0 1
0 1 0	1	0 1
1 0 0	1	0 1
0 1 1	2	1 0
1 0 1	2	1 0
1 1 0	2	1 0
1 1 1	3	1 1

For the inverting adder, the output V_m is given by

$$V_m = -\sum_{j=0}^{N} V_{ij}\frac{C_i}{C_f} + (V_{th}+V_{ss})\left(1+\frac{NC_i}{C_f}\right)$$
$$= -\{nV_H+(N-n)V_L\}\frac{C_i}{C_f}+(V_{th}+V_{ss})\left(1+\frac{NC_i}{C_f}\right), \quad (4)$$

where V_{th}, V_L, V_H and n are the threshold voltage of M1, an input voltage corresponding to logical '0,' an input voltage corresponding to logical '1' and the number of '1' inputs, respectively, and $V_H < V_L < 0$ is assumed. The following relationship should hold for an increment of n to correspond to the level spacing, e/C_g, of the quantizer output:

†The CC load and an oscilloscope are located outside the cryostat housing the SET and the MOSFET for the NDR, and are connected with two 2-m coaxial cables (RG-58C/U).

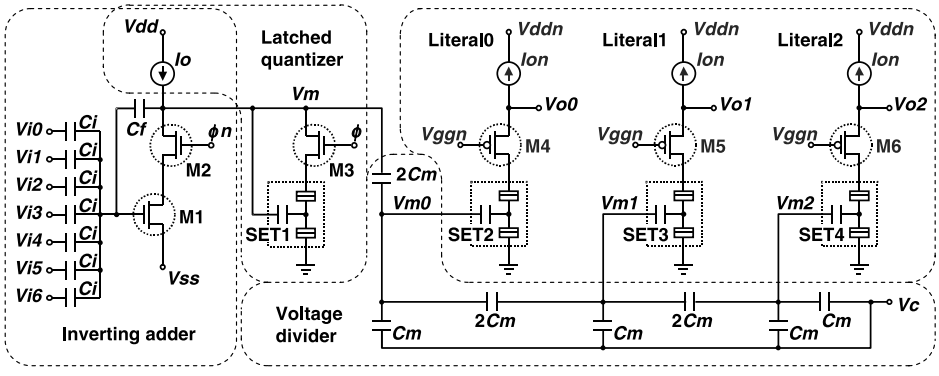

Fig. 7 Circuit diagram of the SET-based 7-3 counter. The circuit consists of five kinds of devices, i.e. single-electron transistors (SET1-4), n-channel MOSFETs (M1-3), p-channel MOSFETs (M4-6), and CC loads for the first stage and the literals. No adjustment is required in the device parameters for devices of the same kind. Clocks ϕ and ϕn are complementary, and the multiple-valued data are latched when ϕ is high. V_{ddn} is set at a negative value to provide consistent voltage levels among the circuit blocks in and out of the counter. Note that the back gate for adjusting the SET characteristics is not required in this configuration.

$$-(V_H - V_L)\frac{C_i}{C_f} = \frac{e}{C_g}, \tag{5}$$

where e and C_g are an electronic charge and the gate capacitance of the SET, respectively.

The stability points for the latched quantizer can be obtained when we consider that the SET oscillation period is e/C_g, the oscillation phase is shifted by nearly half the SET drain voltage, $V_{ds(SET)}$, and the stability points are halfway between the I_d peak and valley on the positive slopes. Thus, the output V_m corresponding to the stability points is expressed as

$$V_m \simeq (1/4 + n + n_o)e/C_g + V_{ds(SET)}/2, \tag{6}$$

where n_o is the number of unused stability points, counting from the first.

By combining (4) through (6) and eliminating n and V_H, $V_{th} + V_{ss}$ of the inverting adder can be expressed as

$$V_{th} + V_{ss} = \{NV_LC_i/C_f + (1/4 + n_o)e/C_g + V_{ds(SET)}/2\}/(1 + NC_i/C_f). \tag{7}$$

For the capacitive voltage divider [13], the outputs V_{m0}, V_{m1} and V_{m2} are related to input V_m as

$$V_{m0} = (V_m - V_c)/2 + V_c, \tag{8}$$

$$V_{m1} = (V_m - V_c)/4 + V_c, \quad \text{and} \tag{9}$$

$$V_{m2} = (V_m - V_c)/8 + V_c. \tag{10}$$

In the periodic literals, output transitions occur at the intersections of SET I_d-V_{gs} characteristics and the load line I_{on}. More specifically, the output of the literal can be made '0' in the 0.25 to $0.75e/C_g$ input range, and '1' between 0.75 and $1.25e/C_g$, when the drain voltage $V'_{ds(SET)}$ is negligible and I_{on} is properly adjusted. The '0' and '1' outputs are repeated alternately with a period of e/C_g. For literal0, literal1 and literal2 to work cooperatively as a counter, each '0' or '1' output range must include one, two, and four $n's$, respectively. Considering that the oscillatory I_d-V_{gs} characteristics of the SETs are shifted in the negative direction by nearly half the absolute drain voltage $|V'_{ds(SET)}|$, the conditions are expressed as

$$V_{m0} \simeq (1/2 + n/2 + n'_o)e/C_g - |V'_{ds(SET)}|/2 \tag{11}$$

$$V_{m1} \simeq (3/8 + n/4 + n'_o)e/C_g - |V'_{ds(SET)}|/2 \tag{12}$$

$$V_{m2} \simeq (5/16 + n/8 + n'_o)e/C_g - |V'_{ds(SET)}|/2. \tag{13}$$

Here, n'_o is the number of oscillatory periods that are not used in periodic literals, counting from the first.

Rearranging (6) and (8) through (13), we obtain the following relationships:

$$V_{ds(SET)} + |V'_{ds(SET)}| = \{1 + 2(n'_o - n_o)\}e/C_g \tag{14}$$

$$V_c = (1/4 + n'_o)e/C_g - |V'_{ds(SET)}|/2 \tag{15}$$

To sustain the Coulomb blockade condition, $V_{ds(SET)}$ and $|V'_{ds(SET)}|$ must be smaller than e/C_Σ ($< e/C_g$), and therefore the right side of Eq. (14) must be minimized. This results in $n_o = n'_o$. Typical conditions are $n_o = n'_o = 1$, $V_{ds(SET)} = |V'_{ds(SET)}| = 0.5e/C_g$, and $V_c = e/C_g$. Note that the SET drain voltages are controlled by MOSFETs and kept nearly at the MOSFET gate voltage minus threshold voltage.

Table 2 Device parameters for simulation. SETs with an oscillation period, e/C_g, of 0.25 V are used together with narrow-channel MOSFETs in the 0.25-μm generation. V_{th} and S are defined at $|I_d| = 100$ nA and $|V_{ds}| = 0.1$ V.

	Temp.	77 K
SET	C_g	0.64 aF
	C_s, C_d	0.18 aF
	R_s, R_d	100 kΩ
MOSFET	L	200 nm
	W	50 nm
	t_{ox}	5 nm
	C_{gdo}, C_{gso}	200 pF/m
	C_{gdl}, C_{gsl}	50 pF/m
	V_{th} } n-ch.	0.91 V
	S } n-ch.	49 mV/dec
	V_{th} } p-ch.	-0.92 V
	S } p-ch.	48 mV/dec

6. Simulation Results

The operation of the proposed 7-3 counter was verified by using a SPICE circuit simulator implemented with the proposed SET model. As shown in Table 2, SETs with an oscillation period, e/C_g, of 0.25 V were used together with narrow-channel MOSFETs in the 0.25-μm generation[†] The small MOSFET is needed in order to reduce the capacitances and consequently increase the operating speed. The short channel may increase the sensitivity of V_{th} to the drain voltage, degrade the cut-off characteristics (subthreshold slope), and decrease the output resistance. These effects may lead to reduced PVCR in the NDR characteristics, and to reduced sharpness (voltage gain) in the transfer curve of the literals, but they are not fatal with the present device sizes. It should also be noted that the effects could be partially alleviated by using narrow-channel devices [14]. The amplitude $|V_H - V_L|$ of the literal output was designed to be 1.0 V ($= 4e/C_g$) to realize margins in V_H and V_L levels, and, consequently, the voltage gain C_i/C_f of the inverting adder was set at 1/4. Ideal CC loads were assumed in the present simulation. The use of a MOSFET with the same dimensions (i.e. L=200 nm, W=50 nm) as a CC load may not be appropriate due to the channel length modulation effect and the low output resistance. The use of longer MOSFETs for a larger output resistance would induce an area penalty, but this could be minimized by improving the device structure [16].

Figure 8 shows the DC input-output characteristics of

[†]0.25-μm generation means that the gate length L, gate oxide thickness t_{ox}, and supply voltage V_{dd} correspond to that generation. However, a channel width W of 50 nm cannot be attained with 0.25-μm technology, but by technology with an MPU/ASIC 1/2 pitch of 50 nm, which is expected to be available in 2009 [15].

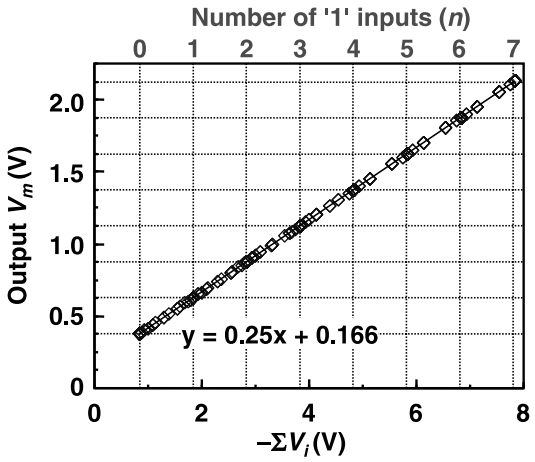

Fig. 8 Simulated input-output characteristics of the inverting adder. C_i = 100 aF, C_f = 400 aF, V_L = −0.12 V, V_H = −1.12 V, ϕn = 1.05 V, V_{dd} = 2.5 V, V_{ss} = −0.85 V, and I_o = 230 nA are assumed.

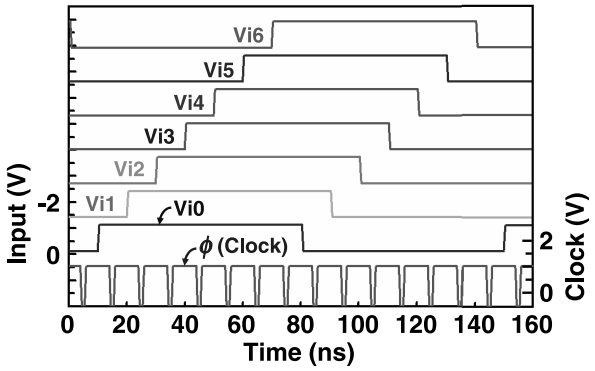

Fig. 9 Waveforms of inputs $V_{i0} \sim V_{i6}$ and clock ϕ. High and low levels of the inputs are −1.12 and −0.12 V, respectively. The clock levels are 1.05 and −0.5 V, respectively. The data are shifted for clarity.

the inverting adder. Output voltages of 1.5 to $8.5e/C_g$ are obtained with sufficient linearity. These voltages are compatible with the quantized voltages in (3) for n_o = 1 and $V_{ds(SET)} = 0.5e/C_g$.

A transient simulation for the combined inverting adder and latched quantizer is performed with input waveforms shown in Fig. 9. The period and width of the clock ϕ for quantizing are 10 and 1 ns, respectively.

Figure 10 shows waveforms of the MV signals corresponding to a ±10% variation in the input amplitudes. Although fluctuations resulting from the input variation can be observed at the leading edges of the stairs where the inverting adder is activated, the stairs are mainly flat and stable at the quantized levels.

Figure 11 compares the input-output characteristics of the periodic literals for negative (a) and positive (b) supply voltages. The input voltages for the first '0' output shift to 0.25 and $0.75e/C_g$, respectively, due to the SET drain voltage $|V_{ds(SET)}|$ of $0.5e/C_g$. It can be seen that the drain voltage and its polarity have a large effect on the phase of the oscillatory characteristics of the literals, and the use of the literal

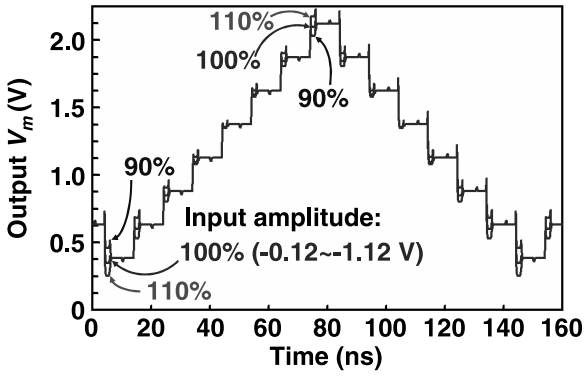

Fig. 10 Simulated output waveforms of the latched quantizer for three combinations of input '1' and '0' levels, −1.12 ∼ −0.12 V (100%), −1.07 ∼ −0.17 V (90%), and −1.17 ∼ −0.07 V (110%). Input amplitude variation of ±10% is cancelled by the quantizer and does not affect the output.

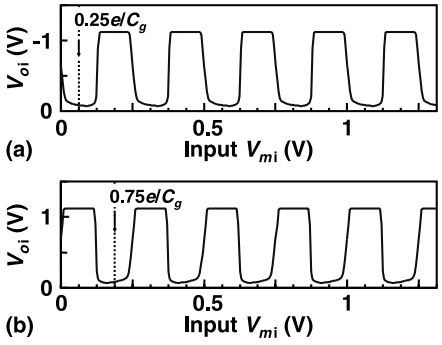

Fig. 11 Simulated input-output characteristics of the SET periodic literals operated with negative (a) and positive (b) supply voltages. Input voltages for the first '0' output are shifted to $0.25e/C_g$ and $0.75e/C_g$, respectively, due to the SET drain voltage $|V_{ds(SET)}|$ of $e/2C_g$.

with a negative supply voltage is the key to realizing counters without a special phase control scheme.

Figure 12 shows the output waveforms for literal0 (a), literal1 (b), and literal2 (c). It can be seen that binary data corresponding to the number of '1' inputs, n, are accurately generated, and the counting operation is performed correctly. The dashed and dotted lines indicate 110% and 90% of the typical amplitude, respectively. Low and high levels of the output signals are within the ±10% variation, and the voltage levels among circuit blocks are consistent.

7. Discussion

To provide a comparison, Fig. 13 shows a conventional 7-3 counter designed only with MOSFETs. Since the SET-based 7-3 counter consists of only 14 devices, including constant-current sources, the number of devices is reduced to less than 1/10 with the SET-based circuit. This dramatic reduction is achieved mainly as a result of the high functionality of the SETs, especially their periodic input-output characteristics and ability to latch MV voltages, and this could lead to a lower power consumption and a higher operation speed.

The power consumption is estimated to be 1.0 μW for the input waveforms in Fig. 9. This is more than two orders of magnitude smaller than those of conventional counters. The low capacitance nature of SETs allows operation with a small current, and their high functionality makes the circuit small, leading to reduced power consumption. This degree of power reduction cannot be realized solely with MOSFETs and this will remain the case even in the future [15].

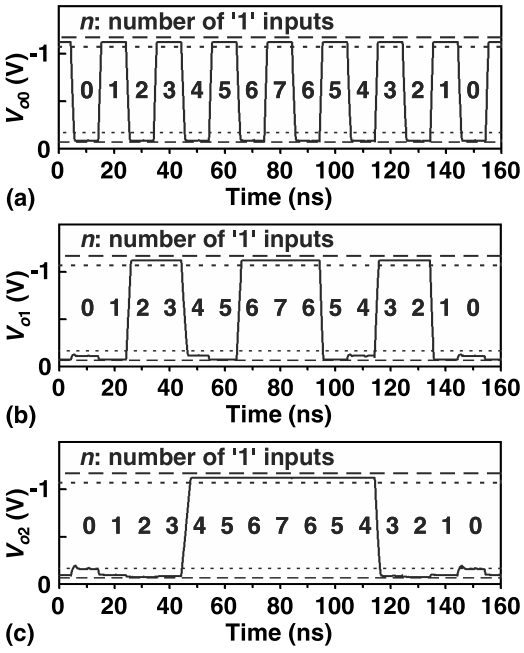

Fig. 12 Simulated output waveforms for literal0 (a), literal1 (b) and literal2 (c) corresponding to the inputs in Fig. 9. $V_{ddn} = -1.12$ V, $V_{ggn} = -1.04$ V, $I_{on} = -170$ nA, $C_m = 100$ aF, and a capacitive load of 100 aF for each output (not shown in Fig. 7) are assumed. Typical output '1' and '0' voltages are −1.12 and −0.12 V, respectively. Dashed and dotted lines indicate 110% and 90% of the typical amplitude, respectively.

The simulated clock frequency of 100 MHz leaves some room for improvement, considering the V_m swing of 1.75 V, the capacitive load of 500 aF, and the current load of 230 nA. However, any attempt at further improvement by reducing capacitances and voltages, and by increasing current, requires a careful consideration of capacitance accuracy and a compromise between the reduced supply voltage and the increased SET drain voltage with limited tunneling conductance ($< e^2/h$).

Control of the MOSFET V_{th} is important for the proposed circuit. In the inverting adder, the deviation of the M1 V_{th} is amplified by the gain, $1 + NC_i/C_f = 2.75$, and appears as an offset voltage in V_m (See Eq. (4)). Since half the level spacing of the quantizer is $0.5e/C_g = 125$ mV, $0.5e/C_g/(1 + NC_i/C_f) = 45$ mV is allowed as the V_{th} deviation. With the cascode MOSFETs, M3-M6, the V_{th} deviation is directly reflected as a change in the SET drain voltage, $V_{ds(SET)}$. Since the target $V_{ds(SET)}$ is $0.5e/C_g = 125$ mV as mentioned in Sect. 5, a V_{th} increase, i.e. $V_{ds(SET)}$ decrease, by $0.25e/C_g = 62.5$ mV will completely destroy the operation of the quantizer and the periodic literals. Even if the V_{th} increase is not very great, the duty ratio of the literal characteristics (See Fig. 11 for example) will be affected. Thus, the acceptable deviation of the V_{th} for the most significant literal, i.e. literal2 with the 7-3 counter, is further reduced by the factor $N + 1 = 8$ and becomes 7.8 mV, if we simply assume that the change in the duty ratio is proportional to that in the V_{th}. Since the absolute V_{th} value is difficult to control to this accuracy, the gate bias V_{ggn} has to be supplied from a circuit consisting of the dummy SET and a MOSFET of the same kind.

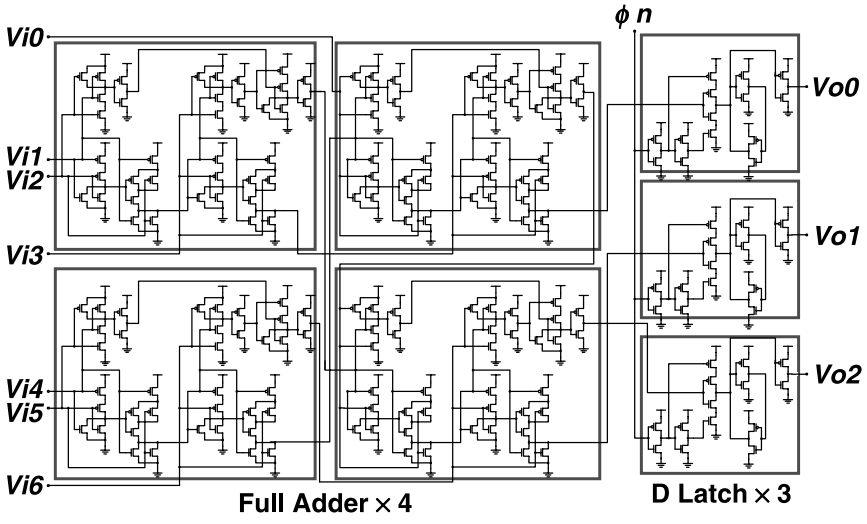

Fig. 13 Conventional 7-3 counter designed only with MOSFETs. Transistor count is 194. Power consumption is estimated to be 360 μW at $V_{dd} = 3.3$ V and $f = 100$ MHz for 0.35-μm devices (equivalently 110 μW in the 0.25-μm generation).

8. Conclusion

A methodology for simulating SET-based MVLs has been introduced. A simple and accurate SET model is implemented in a SPICE circuit simulator, and the parameters are extracted from the measured characteristics of PADOX devices. By using a simulator with the extracted parameters, the experimental data of basic MVL circuits, such as an NDR and a quantizer, can be successfully reproduced. As an advanced example of SET-based logics, a latched parallel counter, which is one of the most important components in arithmetic circuits, was newly designed and analyzed by a simulation. It was found that a SET-based 7-3 counter can be constructed with less than 1/10 the usual number of devices and can operate at a moderate speed ($\simeq$100 MHz) with 1/100 the power consumption of a conventional circuit. These results indicate the usefulness of the proposed methodology, and the great potential for SET-based MVL especially in terms of low-power operation and reduced circuit size.

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