PAPER Special Section on New System Paradigms for Integrated Electronics

A Single-Electron-Transistor Logic Gate Family for Binary, Multiple-Valued and Mixed-Mode Logic

Katsuhiko DEGAWA[†a)], ***Student Member***, **Takafumi AOKI**[†], ***Member***, **Tatsuo HIGUCHI**[††], ***Fellow***, **Hiroshi INOKAWA**[†††], ***and*** **Yasuo TAKAHASHI**[††††], ***Members***

SUMMARY This paper presents a model-based study of SET (Single-Electron-Transistor) logic gate family for synthesizing binary, MV (Multiple-Valued) and mixed-mode logic circuits. The use of SETs combined with MOS transistors allows compact realization of basic logic functions that exhibit periodic transfer characteristics. The operation of basic SET logic gates is successfully confirmed through SPICE circuit simulation based on the physical device model of SETs. The proposed SET logic gates are useful for implementing binary logic circuits, MV logic circuits and binary-MV mixed-mode logic circuits in a highly flexible manner. As an example, this paper describes design of various parallel counters for carry-propagation-free arithmetic, where MV signals are effectively used to achieve higher functionality with lower hardware complexity.

key words: *single-electron transistors, multiple-valued logic, quantum devices, logic circuits, parallel counters*

1. Introduction

Advances in integrated circuit technology have been based mostly on CMOS circuit technology operating on the basis of binary logic. However, major problems in present-day LSI technology, such as increased power consumption, interconnect delay, limited integration density and device scaling limits, cannot be addressed simply by improving the conventional CMOS technology. An advanced device/circuit technology that achieves higher functionality with fewer hardware components will be desirable in the next-generation low-power System-on-Chip (SoC) architecture.

Emerging single-electron devices, especially Single-Electron Transistors (SETs) [1], [2], have a possibility of achieving high functional density and extremely low power operation in principle. For practical applications, however, we must make clear what kinds of new functionality could be supported by SETs and how the emerging functionality will be applied to useful computation. As a first step to address these questions, in this paper, we present a model-based analysis of possible SET logic gates and their potential functionality in synthesizing binary, MV (Multiple-Valued) and mixed-mode logic circuits. The operation of basic SET logic gates is successfully confirmed through SPICE circuit simulation based on the physical device model of SETs [3].

The use of SETs combined with MOS transistors [4], [5] allows compact realization of basic logic functions that exhibit periodic transfer characteristics, whose amplitude, period and phase can be programmed independently. This unique property is particularly useful for implementing binary logic circuits, MV logic circuits and binary-MV mixed-mode logic circuits. On the basis of this idea, we also discuss application of the proposed SET logic gates to the implementation of carry-propagation-free arithmetic circuits. We demonstrate that the use of SETs makes possible extremely compact realization of parallel counter (or adder) circuits required for high-speed arithmetic.

2. Basic Logic Gates Using SETs

2.1 Mathematical Notation

We first define the basic mathematical notation of logic operators used in the following discussion. Let L_r be the set of logic values in r-valued logic, which is defined as $L_r = \{0, 1, \cdots, r-1\}$ $(r \geq 2)$. As a special case, binary logic assumes the logic value set $L_2 = \{0, 1\}$. We use binary-logic operators $\wedge$ (AND), $\vee$ (OR), $\oplus$ (EXOR) and $^-$ (NOT), which are defined on L_2.

In order to discuss the realization of r-valued logic function, we need to define *linear summation* $+$ on L_r, where the logic values $0, 1, \cdots, r-1$ are regarded as integer numbers. Also, we define *literal* operator x^S over the r-valued variable $x(\in L_r)$ as

$$x^S = \begin{cases} 1 & \text{if } x \in S \\ 0 & \text{otherwise,} \end{cases}$$

where $S \subseteq L_r$. Note that the literal operator is a mapping $L_r \to L_2$.

2.2 SET Logic Gates

The SET is the most fundamental of various single-electron devices. The SET must have a small conductive island to

Manuscript received May 1, 2004.
Manuscript revised July 15, 2004.

[†]The authors are with the Department of Computer and Mathematical Sciences, Graduate School of Information Sciences, Tohoku University, Sendai-shi, 980-8579 Japan.
[††]The author is with the Department of Electronics, Faculty of Engineering, Tohoku Institute of Technology, Sendai-shi, 982-8577 Japan.
[†††]The author is with NTT Basic Research Laboratories, NTT Corporation, Atsugi-shi, 243-0198 Japan.
[††††]The author is with the Graduate School of Information Science and Technology, Hokkaido University, Sapporo-shi, 060-0814 Japan.
a) E-mail: degawa@aoki.ecei.tohoku.ac.jp

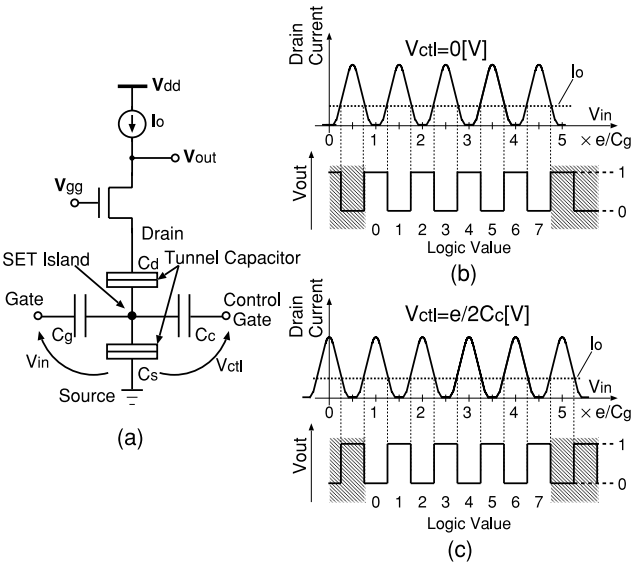

Fig. 1 SET periodic literal circuit: (a) schematic, (b) transfer characteristics when $V_{ctl} = 0$ [V] and when (c) $V_{ctl} = \frac{e}{2C_c}$ [V].

exploit the Coulomb blockade for manipulating electrons by means of one-by-one transfer.

Figure 1(a) shows a schematic of a *periodic literal* circuit, which consists of a SET, a MOSFET and a Constant-Current (CC) load I_o. The SET has an input gate and a control gate that controls the phase of periodic waveform of drain current. The MOSFET with a fixed gate bias of V_{gg} is used to keep the SET drain voltage almost constant at $V_{gg} - V_{th}$, where V_{th} is the MOSFET threshold voltage. The $V_{gg} - V_{th}$ is set low enough to sustain the Coulomb blockade condition. In addition, the MOSFET works as a cascode device and keeps the output resistance of the circuit high. The current through this circuit increases and decreases periodically as a function of input voltage unless the CC load is connected. The current is determined only by the input voltage; it is independent of the output voltage, because the drain voltage of the SET is kept constant by the MOSFET. When the CC load is connected and the increasing drain current crosses the load line of I_o, the output voltage V_{out} switches very sharply from high to low. On the other hand, when the decreasing drain current crosses the load line, the output voltage switches from low to high.

We assume discrete logical levels (or logic values) corresponding to specific voltage levels as shown in Figs. 1(b) and (c) for the case of $r = 8$. The output V_{out} becomes logical "1" when the SET is off and V_{out} becomes "0" when the SET is on. The periodic waveform of the output is shifted by half period by applying a constant dc voltage $V_{ctl} = \frac{e}{C_c}$ [V] (logical 1), where C_c is the capacitance of the control gate. The waveform shift due to the control-gate potential is illustrated in Fig. 1(b) (when V_{ctl} is logical 0) and (c) (when V_{ctl} is logical 1). As a result, Fig. 1(b) realizes the literal function $x^{\{0,2,4,6\}}$, and (c) realizes $x^{\{1,3,5,7\}}$

Figure 2 shows a family of possible logic gates using SETs for realizing binary logic, MV (Multiple-Valued) logic and mixed-mode logic circuits. As described above, the SET periodic literal could be used to discriminate MV signals (including binary signals as a special case) using a binary periodic waveform. We can consider two types of circuit configuration for the SET periodic literal, i.e., CC-load type and complementary type as illustrated in Fig. 2. (In the complementary-type configuration, SET A and SET A' must be designed to switch in a complementary manner.) For both types, we can shift the phase of periodic output by changing the potential applied to the control gate. Thus, we have two different transfer characteristics of periodic literals depending on the potential of the control gate ($a = 0$ or $a = 1$). Let S_0 and S_1 denote the set of even logic values $\{0, 2, 4, \cdots\}(\subseteq L_r)$ and the set of odd logic values $\{1, 3, 5, \cdots\}(\subseteq L_r)$, respectively. The resulting function of the periodic literal circuit corresponds to x^{S_0} when $a = 0$ and to x^{S_1} when $a = 1$. Assuming the use in binary logic ($r = 2$), the two parameter settings $a = 0$ and $a = 1$ correspond to negative and positive literals, $x^{\{0\}} = \bar{x}$ and $x^{\{1\}} = x$, respectively, as shown in Fig. 3(a).

Also, we propose three different two-input logic gates, i.e., a *parallel gate*, a *series gate* and a *summing gate*, as shown in Fig. 2. For every two-input logic gate, we could consider CC-load-type and complementary-type configurations. These two-input gates could accept MV signals. The equivalent function of the parallel (or series) gate is represented by an AND (or OR) connection of a pair of periodic literals as shown in Fig. 2. Another interesting property of the parallel (or series) gate is that its function could be programmed by the potential applied to the control gates $a, b(\in \{0, 1\})$ in a highly flexible manner. As a result, the function of parallel gate is represented by $x^{S_a} \wedge y^{S_b}$ and that of series gate is $x^{S_a} \vee y^{S_b}$. Assuming the use in binary logic, there are possible four functions for every parallel (or series) gate corresponding to the parameters $(a, b) = (0, 0), (0, 1), (1, 0), (1, 1)$ as shown in Figs. 3(b) and (c).

On the other hand, the two-input summing gate employs an unique structure for capacitive voltage addition as shown in the last column of Fig. 2. The function of the summing gate can be represented as $(x + y)^{S_a}$. For binary logic ($r = 2$), the function can be rewritten as

$$(x+y)^{S_a} = \begin{cases} (x+y)^{\{0,2\}} = \overline{x \oplus y} & \text{if } a = 0 \\ (x+y)^{\{1\}} = x \oplus y & \text{if } a = 1. \end{cases}$$

Thus, the summing gate is particularly useful for implementing EXNOR ($a = 0$) and EXOR ($a = 1$) operations as illustrated in Fig. 3(d).

Other useful logic gates are listed in Fig. 4. The inverting adder is used to combine plural binary (or MV) signals into a single MV signal, where the inputs must have negative polarity. The SET periodic literal with negative output, which is also listed in Fig. 4, is used to provide negative input signals for the inverting adder. The voltage divider, on the other hand, is used to scale the voltage applied to the SET so as to change the period of square-wave transfer characteristics. The latched quantizer is used as an MV memory whose output is quantized to have discrete logic levels.

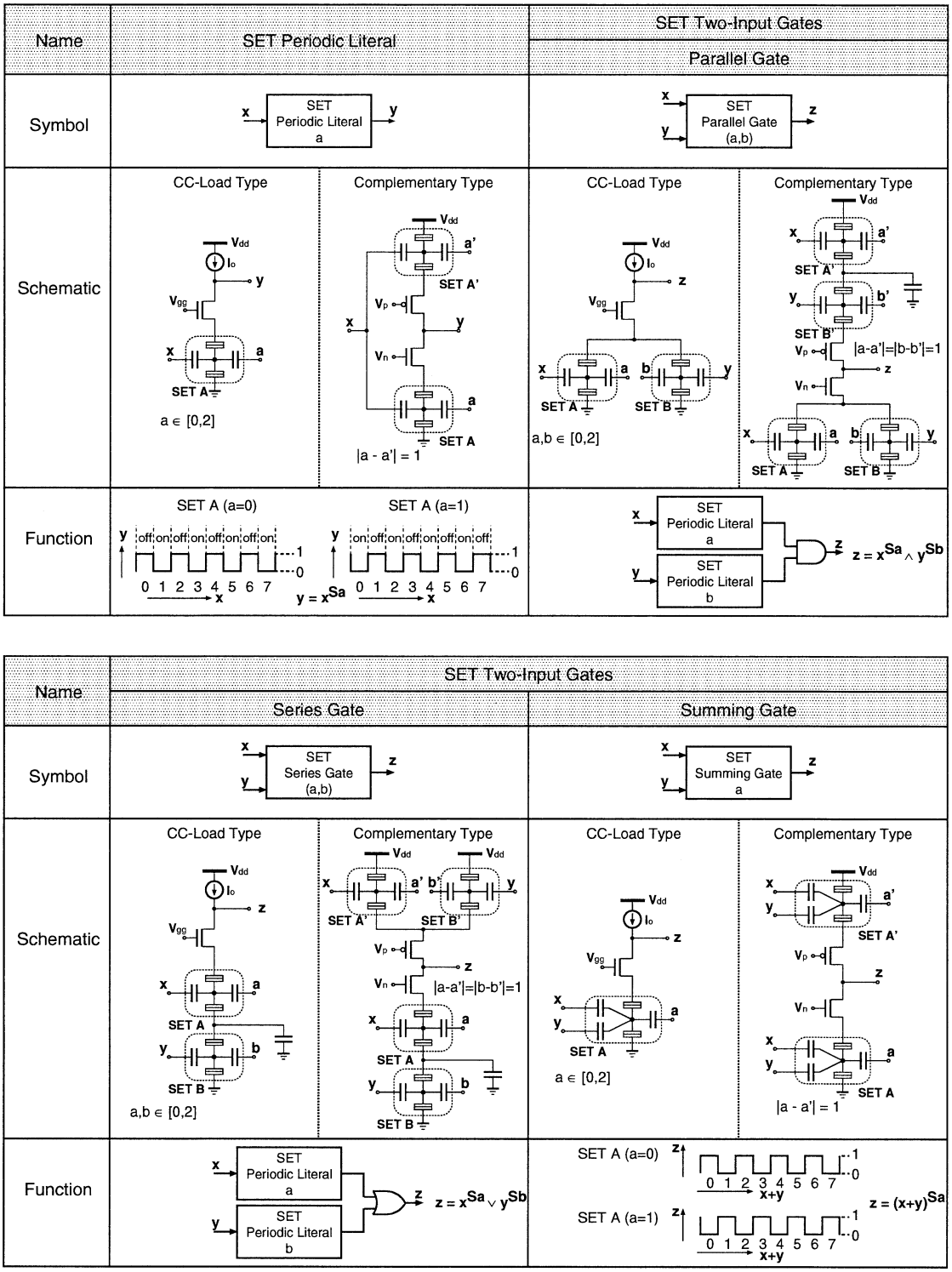

Fig. 2 SET logic gate family: SET periodic literals and SET two-input gates.

2.3 Simulation Examples of SET Logic Gates

We confirmed the basic operation of the proposed SET logic gates shown in Fig. 2 by the SPICE simulation. The analytical device model of the SET reported in [3] is used for the SPICE simulation. The SET model is based on the steady-state master equation and takes only the two most-probable charging states into account. The model is implemented to SmartSpice [6] as a subcircuit comprising analog behavioral devices.

Table 1 shows device parameters used for circuit simu-

lation, where we assume the use of two different power supply voltages; V_{DD} is for the MV operation and V_{dd} is for the binary operation. For the MV operation, we assume four-valued inputs $\{GND, V_{dd}, 2V_{dd}, 3V_{dd}(= V_{DD})\}$ corresponding to four logical values {0, 1, 2, 3}, respectively. The channel width $W = 50$ nm of the MOSFET in Table 1 might be quite small when assuming the present state of technology. In future, however, such device geometry will become available as predicted in ITRS roadmap [7]. Also, special device structures such as FinFET [8] may provide a reasonable way of fabricating narrow-channel-width MOSFETs. But, of course we need to address many technical problems, including problems of process variation, in realizing 50 nm channel width. Because of the device model constraint, every terminal of SET should be driven by a constant-voltage source or should be connected to a capacitor whose value is much larger than the total capacitance $C_{total}(= C_g+C_b+C_d+C_s)$ of the SET. In most of our simulations, the terminals of SETs are connected to constant-voltage sources. In the case of series-connected gates, on the other hand, we attached a 30 aF capacitance at every series connection point, where 30 aF is larger than C_{total} (= 0.9 aF).

Figure 5 shows the simulation results of the SET periodic literals. We simulated both "CC-load type" and "complementary type" circuit configurations with different settings of control gate voltages. In simulations of CC-load-type gates, we used ideal current sources as constant-current

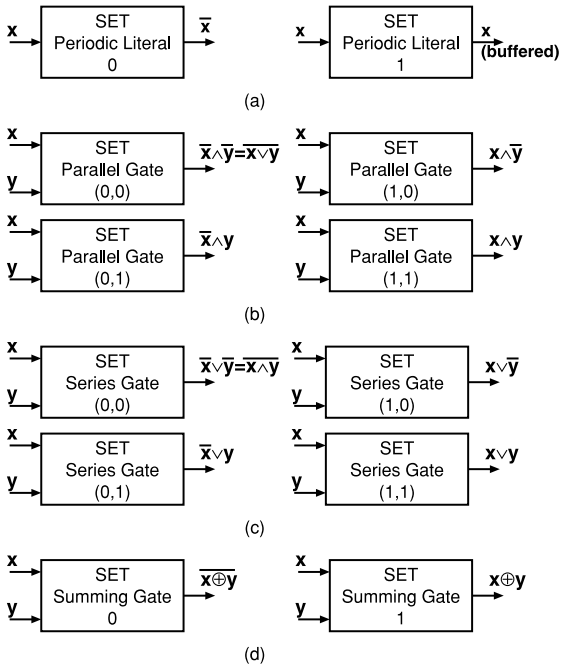

Fig. 3 Equivalent binary logic functions of SET logic gates.

Table 1 Device parameters for SPICE simulations.

	Temperature	100 K
SET	C_g, C_b	0.27 aF
	C_s, C_d	0.18 aF
	R_s, R_d	100 kΩ
MOSFET	L	200 nm
	W	50 nm
	t_{ox}	5 nm
	C_{gdo}, C_{gso}	200 pF/m
	C_{gdl}, C_{gsl}	50 pF/m
	V_{th}	0.87 V
	S	54 mV/dev
Bias & Load	V_{DD}	0.9 V
	V_{dd}	0.3 V
	V_{gg}	0.95 V
	I_o	75–80 nA
	C_L	0.1 fF

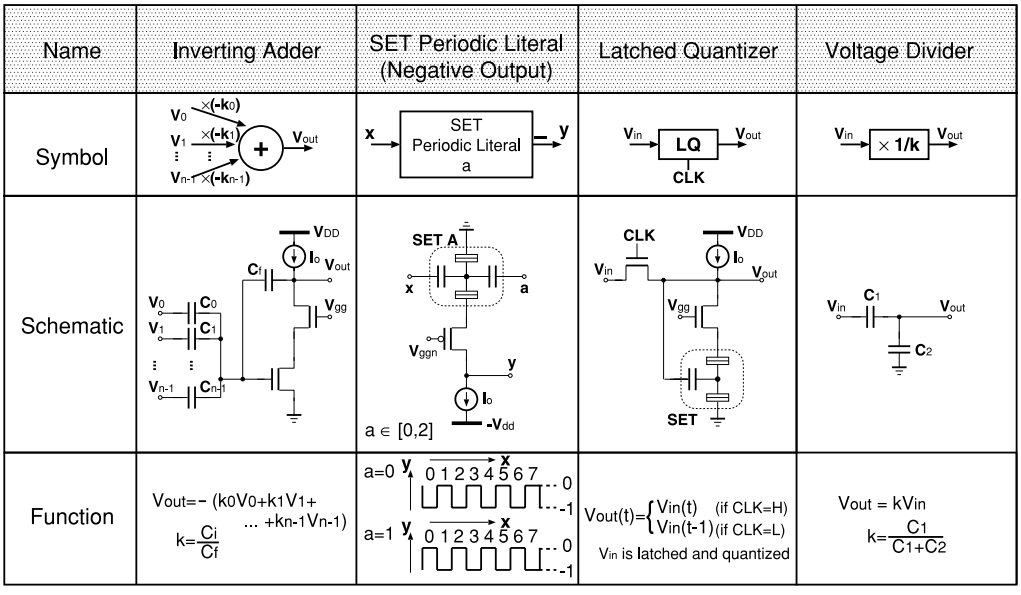

Fig. 4 SET logic gate family: additional components.

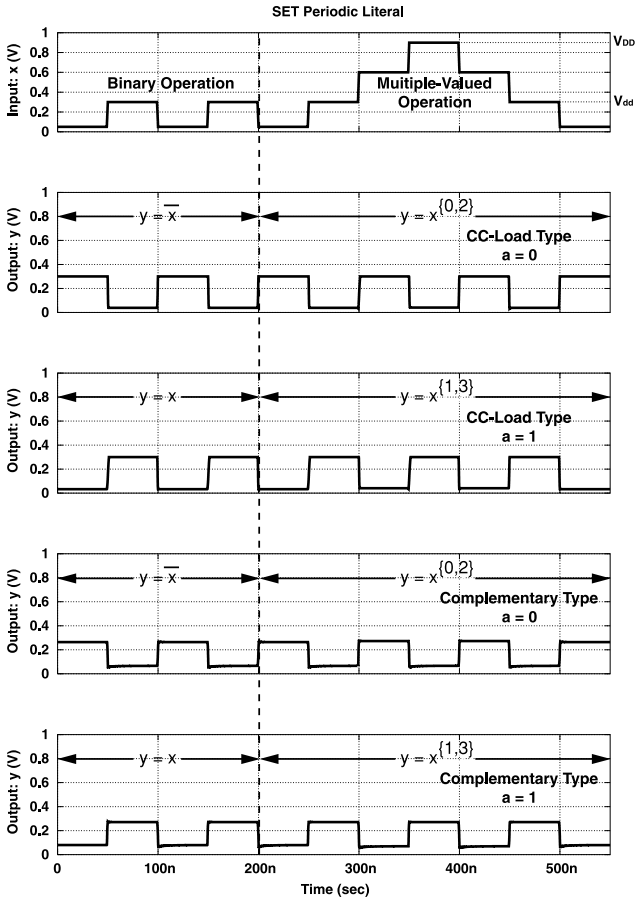

Fig. 5 SPICE simulation results of SET periodic literals (the CC-load type and the complementary type).

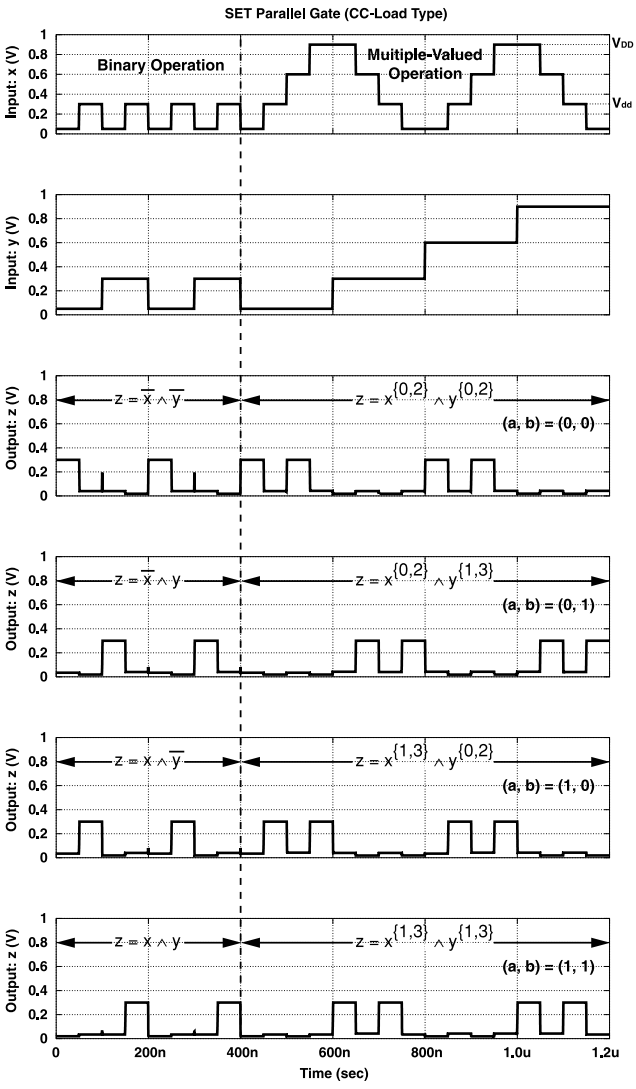

Fig. 6 SPICE simulation results of the SET parallel gate (CC-load type).

loads. In practice, the constant-current loads could be implemented by MOSFETs, where we should consider the effect of channel-length modulation and the output resistance of the MOSFET CC load. To suppress the effect of channel-length modulation and to maintain the sufficient level of output resistance, we need to employ MOSFETs whose channel lengths are 2–3 times larger than the minimum geometry. This situation may become worse in future as device size shrinks. Addressing this problem, advanced device structures, such as reported in [7], should be introduced to improve the MOSFET characteristics. The correct operation is successfully confirmed for binary input signals (0–200 ns) and also for four-valued input signals (200–550 ns).

Figures 6 and 7 show the simulated waveforms for the parallel gate and series gate, respectively. Though the figure shows only the result of "CC-load type" configuration, we verified correct operation of both "CC-load type" and "complementary type" configurations for all the possible parameters (a, b). Similarly, simulation examples of the summing gate are shown in Fig. 8. As is observed in these results, we can conclude that the proposed SET logic gates provide highly flexible functionality not only for binary input signals but also for MV input signals. Note that all these gates produce binary output signals. To produce MV signals, we need to employ the additional components shown in Fig. 4. We also verified correct operation of these components through extensive SPICE simulation. Additionally, we designed and simulated a five-stage ring oscillator consisting of five SET periodic literal gates. Assuming a 20 aF load for each gate, the oscillation frequency was 625 MHz in this simulation.

The detailed simulation results of complete application circuits (including the additional components) can be found in our conference papers [5], [8], [9] and the subsequent paper [10] submitted in this special issue (the paper is focused on the simulation methodology of SET logic circuits of practical size).

On the other hand, main focus of this paper is to propose a family of basic SET logic gates and to show its functional completeness in synthesizing binary and MV logic circuits as is discussed the following sections.

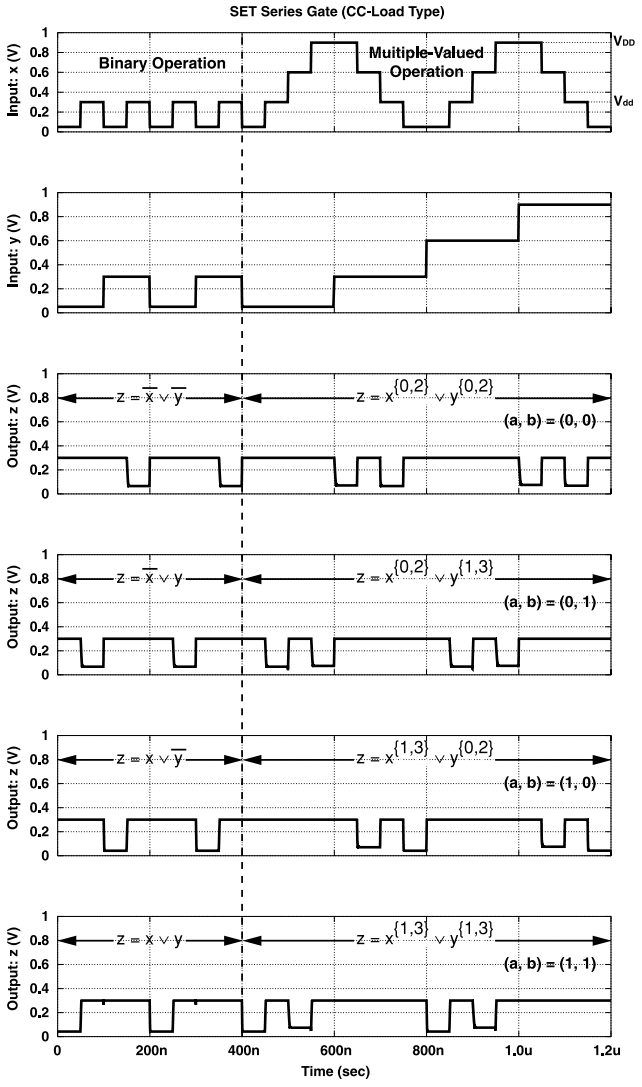

Fig. 7 SPICE simulation results of the SET series gate (CC-load type).

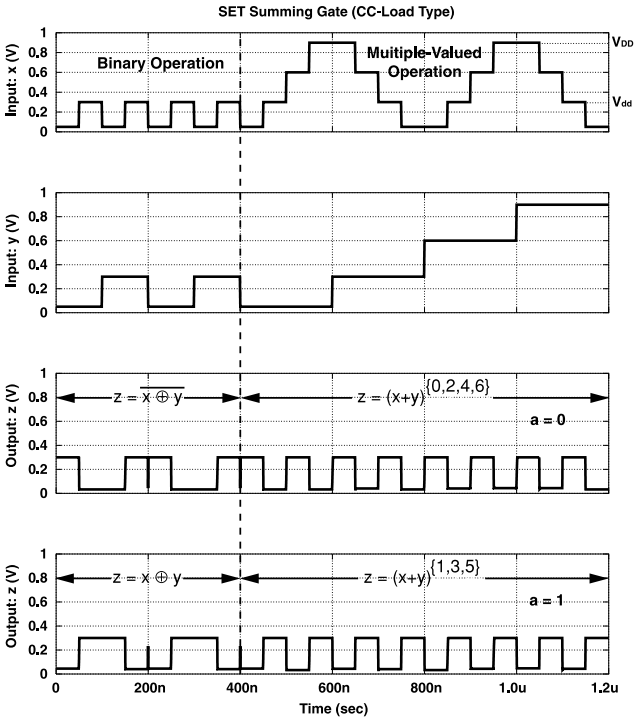

Fig. 8 SPICE simulation results of the SET summing gate (CC-load type).

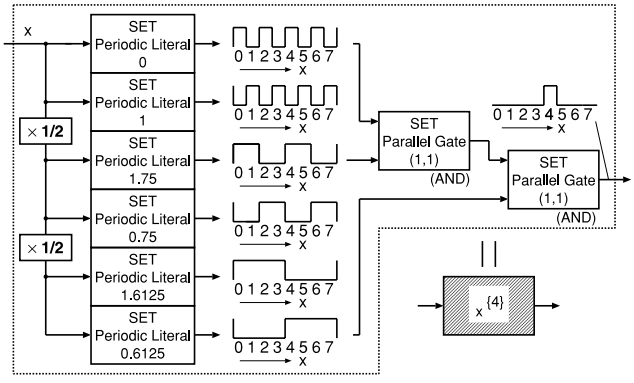

Fig. 9 Realization of the delta literal $x^{\{4\}}$.

3. Realization of Functions in Binary and Multiple-Valued (MV) Logic

3.1 Binary Logic Functions

The proposed SET logic gate family is functionally complete in realizing arbitrary binary logic functions. We can easily confirm this fact from Fig. 3. When $(a, b) = (0, 0)$, the SET parallel gate performs NOR operation.

3.2 Literal Functions for MV Logic

The SET logic gate family is particularly useful for realizing the literal functions with periodic transfer characteristics. In this section, we show that the SET logic gates can realize arbitrary literal functions x^S in principle.

We first consider the realization of delta literal functions x^S with $|S| = 1$, where $|S|$ denotes the number of elements in the set S. Figure 9 shows a typical structure for a delta literal function, where the delta literal $x^{\{4\}}$ in 8-valued logic system is considered as an example. The voltage dividers are used to change the period of SET periodic literals. Then, combining three square-wave literals of different periods using SET parallel gates (AND gates), we can create arbitrary delta-literal functions as shown in Fig. 9. Also, by taking the OR of delta literal functions with SET series gates, we have arbitrary literal functions. Figure 10 shows an example of the literal $x^{\{1,4,5,7\}}$.

3.3 MV Logic Functions

Any MV logic functions of a single variable can be realized by adding the outputs of literal functions as illustrated in Fig. 11. The corresponding 8-valued single-variable logic

function $f(x)$ is represented by

$$f(x) = x^{\{2,4,7\}} + x^{\{2,4,6\}} + x^{\{0,2,3,6\}},$$

where $x, f \in L_8$. Note that the addition is performed by an inverting adder shown in Fig. 4, which could accept only negative signals. Hence, the SET periodic literal with negative output shown in Fig. 4 is used to produce negative binary signals. This approach can be easily extended to the realization of arbitrary MV logic functions of n variables. Figure 12 illustrates a realization of the two-variable function:

$$f(x_1, x_2) = x_1^{\{2,4,7\}} \wedge x_2^{\{2,4,6\}} + x_1^{\{0,2,3\}} \wedge x_2^{\{1,4,5\}},$$

as an example ($x_1, x_2, f \in L_8$). In general, r-valued logic function of n variables can be expressed in the form:

$$f(x_1, x_2, \cdots, x_n) = \sum_i x_1^{S_{i1}} \wedge x_2^{S_{i2}} \wedge \cdots \wedge x_n^{S_{in}},$$

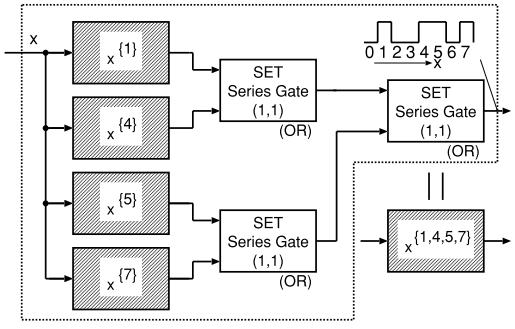

Fig. 10 Realization of the literal $x^{\{1,4,5,7\}}$.

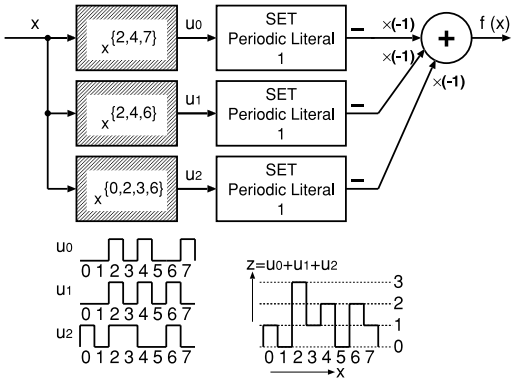

Fig. 11 Realization of an MV logic function of a single variable.

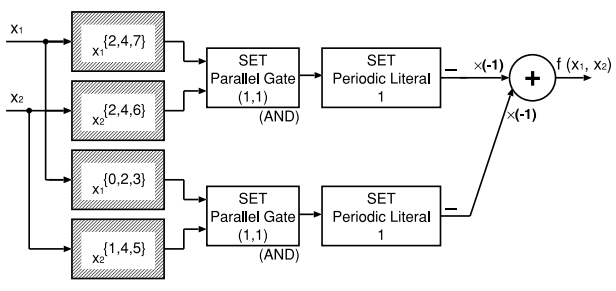

Fig. 12 Realization of an MV logic function of two variables.

where $x_1, x_2, \cdots, x_n, f \in L_r$, $S_{ij} \subseteq L_r$ and $\sum$ denotes the linear summation of the product terms.

As discussed in this section, the proposed SET logic gate family can be used to implement arbitrary binary logic circuits and MV logic circuits. Listed below are important characteristics of the SET logic gates:

- The use of SETs allows extremely simple realization of literal functions with periodic transfer characteristics, which may be useful for designing arithmetic circuits and analog-digital interface circuits.
- The SET can accept MV signals directly to produce binary output. Also, highly compact realization of MV memory is available using the latched quantizer in Fig. 4 [5]. These properties are particularly useful for implementing binary-MV mixed-mode logic circuits and logic-in-memory circuits [11].

4. Design of Parallel Counters for Arithmetic Datapaths

This section describes the SET-based design of parallel counter circuits for carry-propagation-free arithmetic. We give a simple design example of binary-MV mixed-mode logic circuits.

As described in Ref. [12], most of the adders including redundant-number adders could be represented as generalized counters in the framework of Counter Tree Diagrams (CTDs). Thus, such a generalized counter is considered to be one of the most important components in arithmetic circuits. Figure 13 shows a simple example of a binary n-m counter, where $n = 2^m - 1$ in general. The function of the n-m parallel counter can be represented as

$$2^0 y_0 + 2^1 y_1 + \cdots + 2^{m-1} y_{m-1} = x_0 + x_1 + \cdots + x_{n-1}.$$

The n-m parallel counter counts the number of 1s in the input signals as follows: (i) add the n binary signals to an $(n+1)$-valued signal $[0:n]$, and (ii) decompose the $(n+1)$-valued signal to m binary signals as in the case of analog-to-digital converters.

Figure 14 shows a SET-based implementation of a 3–2 parallel counter. For the first-stage addition, an inverting adder is used, and hence we adopt negative logic for the input/output signals to simplify the circuit configuration. The four-valued signal thus generated is quantized by the latched quantizer, and is decomposed into binary signals by using a pair of periodic literals. Thus, the "counting" operation is

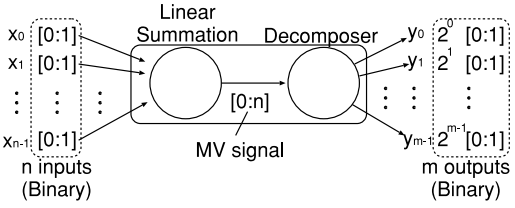

Fig. 13 Binary n-m parallel counter.

directly implemented by a pair of periodic literals without additional components.

The idea of using the periodic transfer characteristics of SETs for the "counting" operation can be naturally extended to higher levels of quantization. Figure 15 illustrates an example of a 7–3 parallel counter, where three periodic literals are employed for converting the 8-valued signal to binary signals. Compared with the ordinary binary implementation, the circuit exhibits extremely simple structure. The detailed circuit design is described in the subsequent paper [10] submitted to this special issue. Our initial observation shows that the SET-based 7–3 counter can be constructed with only 1/14 of devices, and can operate at a moderate speed with 1/100 of power consumption, compared with the conventional CMOS logic implementation.

The multiple-operand parallel counters thus designed are useful for implementing various arithmetic circuits that require multiple-operand addition. For example, Fig. 16 shows the overall architecture of a 32×32-bit pipelined multiplier using parallel counters. The use of 7–3 parallel counters makes possible the reduction in the number of counter stages by 33% and the number of counters by 64%, compared with 3–2 counter-based design.

The above mentioned design principle could be applied to other designs of various parallel adders including the adders in redundant number systems and high-radix number systems. For example, Fig. 17 shows the structure of a radix-2 Positive Digit (PD) adder [13] using 3-valued digits. The circuit configuration is similar to those of parallel counters. Our initial observation in these examples shows that the proposed SET logic gate family is useful for designing binary logic, MV logic and mixed-mode logic circuits.

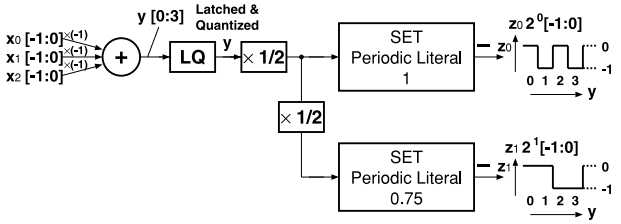

Fig. 14 Realization of the 3–2 parallel counter.

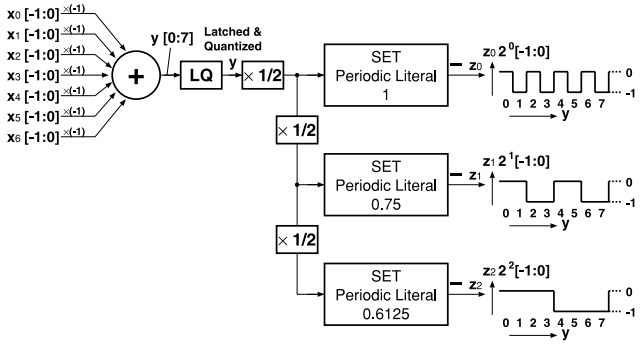

Fig. 15 Realization of the 7–3 parallel counter.

5. Conclusion and Future Prospects

In this paper, we proposed basic SET logic gates useful for

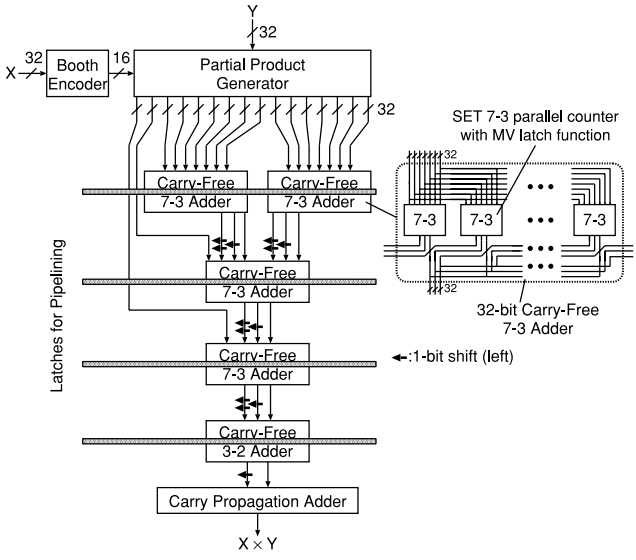

Fig. 16 32 × 32-bit pipelined multiplier using 7–3 parallel counters.

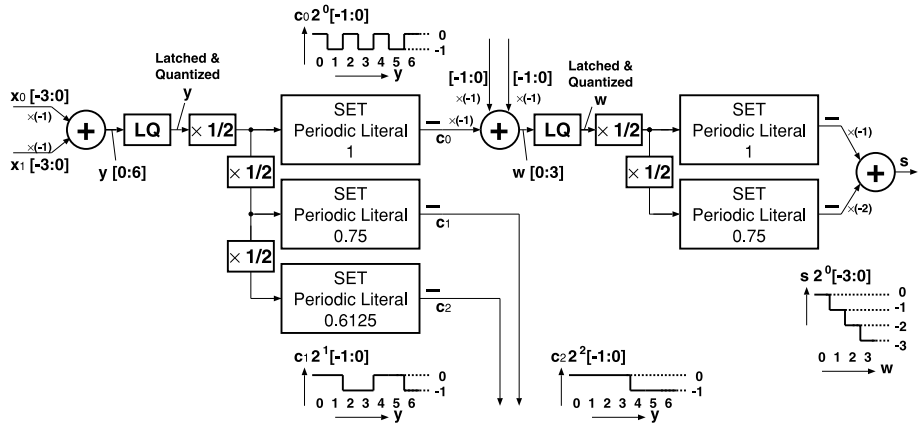

Fig. 17 Realization of the radix-2 PD adder.

designing binary logic, MV logic and mixed-mode logic circuits. The proposed SET logic gate family seems useful in many applications, where low-power area-efficient circuit implementation of mixed-signal interface is essential. Such applications may include logic-in-memory circuits, functional memory systems, Field-Programmable Gate Arrays (FPGAs), computational sensors with on-chip signal processing capability (such as computational image sensors and intelligent chemical/biological sensors), advanced smart dust, signal processors for mobile devices, etc.

References

[1] K.K. Likharev, "Single-electron devices and their applications," Proc. IEEE, vol.87, pp.606–632, April 1999.
[2] Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa, "Silicon single-electron devices," J. Phys., Condens. Matter, vol.14, no.39, pp.R995–R1033, Oct. 2002.
[3] H. Inokawa and Y. Takahashi, "A compact analytical model for asymmetric single-electron tunneling transistors," IEEE Trans. Electron Devices, vol.50, no.2, pp.455–461, Feb. 2003.
[4] H. Inokawa, A. Fujiwara, and Y. Takahashi, "A multiple-valued logic and memory with combined single-electron and metal-oxide-semiconductor transistors," IEEE Trans. Electron Devices, vol.50, no.2, pp.462–470, Feb. 2003.
[5] H. Inokawa and Y. Takahashi, "Experimental and simulation studies of single-electron-transistor-based multiple-valued logic," Proc. 33rd IEEE Int. Symp. on Multiple-Valued Logic, pp.259–266, May 2003.
[6] SILVACO International, Santa Clara, CA, USA.
[7] M. Miyamoto, K. Toyota, K. Seki, and T. Nagano, "An asymmetrically doped buried-layer (ADB) structure for low-voltage mixed analog-digital CMOS LSI's," IEEE Trans. Electron Devices, vol.46, no.8, pp.1699–1704, Aug. 1999.
[8] K. Degawa, T. Aoki, T. Higuchi, H. Inokawa, and Y. Takahashi, "A single-electron-transistor logic gate family and its application—Part I: Basic components for binary, multiple-valued and mixed-mode logic," Proc. 34th IEEE Int. Symp. on Multiple-Valued Logic, pp.262–268, May 2004.
[9] H. Inokawa, Y. Takahashi, K. Degawa, T. Aoki, and T. Higuchi, "A single-electron-transistor logic gate family and its application—Part II: Design and simulation of a 7-3 parallel counter with a linear summation and MV latch functions," Proc. 34th IEEE Int. Symp. on Multiple-Valued Logic, pp.269–274, May 2004.
[10] H. Inokawa, Y. Takahashi, K. Degawa, T. Aoki, and T. Higuchi, "A simulation methodology for single-electron multiple-valued logics and its application to a latched parallel counter," IEICE Trans. Electron., vol.E87-C, no.11, pp.1818–1826, Nov. 2004.
[11] T. Hanyu and M. Kameyama, "Multiple-valued logic-in-memory VLSI architecture based on floating-gate-MOS pass-transistor logic," IEICE Trans. Electron., vol.E82-C, no.9, pp.1662–1668, Sept. 1999.
[12] J. Sakiyama, N. Homma, T. Aoki, and T. Higuchi, "Counter tree diagrams: A unified framework for analyzing fast addition algorithms," IEICE Trans. Fundamentals, vol.E86-A, no.12 pp.3009–3019, Dec. 2003.
[13] S. Kawahito, M. Ishida, T. Nakamura, M. Kameyama, and T. Higuchi, "High-speed area-efficient multiplier design using multiple-valued current-mode circuits," IEEE Trans. Comput., vol.43, no.1, pp.34–42, Jan. 1994.

Katsuhiko Degawa received the B.E. degree in information engineering and the M.S. degree in information sciences from Tohoku University, Sendai, Japan, in 2002 and 2004, respectively. He is currently working towards the Ph.D. degree at Tohoku University. His research interests include new paradigm VLSI computing based on multiple-valued logic. Mr. Degawa received the Tohoku Section Presentation Award from the Institute of Electrical Engineers of Japan in 2002.

Takafumi Aoki received the B.E., M.E., and D.E. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1988, 1990, and 1992, respectively. He is currently a Professor of the Graduate School of Information Sciences at Tohoku University. For 1997–1999, he also joined the PRESTO project, Japan Science and Technology Corporation (JST). His research interests include theoretical aspects of computation, VLSI computing structures for signal and image processing, multiple-valued logic, and biomolecular computing. Dr. Aoki received the Outstanding Paper Award at the 1990, 2000 and 2001 IEEE International Symposiums on Multiple-Valued Logic, the Outstanding Transactions Paper Award from the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan in 1989 and 1997, the IEE Ambrose Fleming Premium Award in 1994, the IEICE Inose Award in 1997, the IEE Mountbatten Premium Award in 1999, and the Best Paper Award at the 1999 IEEE International Symposium on Intelligent Signal Processing and Communication Systems.

Tatsuo Higuchi received the B.E., M.E., and D.E. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1962, 1964, and 1969, respectively. He is currently a Professor at Tohoku Institute of Technology and a Emeritus Professor at Tohoku University. From 1980 to 1993, he was a Professor in the Department of Electronic Engineering at Tohoku University. He was a Professor from 1994 to 2003, and was Dean from 1994 to 1998 in the Graduate School of Information Sciences at Tohoku University. His general research interests include the design of 1-D and multi-D digital filters, linear time-varying system theory, fractals and chaos in digital signal processing, VLSI computing structures for signal and image processing, multiple-valued ICs, multiwave opto-electronic ICs, and biomolecular computing. Dr. Higuchi received the Outstanding Paper Awards at the 1985, 1986, 1988, 1990, 2000 and 2001 IEEE International Symposiums on Multiple-Valued Logic, the Certificate of Appreciation in 2003 and the Long Service Award in 2004 on Multiple Valued Logic, the Outstanding Transactions Paper Award from the Society of Instrument and Control Engineers (SICE) of Japan in 1984, the Technically Excellent Award from SICE in 1986, and the Outstanding Book Award from SICE in 1996, the Outstanding Transactions Paper Award from the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan in 1990 and 1997, the Inose Award from IEICE in 1997, the Technically Excellent Award from the Robotics Society of Japan in 1990, the IEE Ambrose Fleming Premium Award in 1994, the Outstanding Book Award from the Japanese Society for Engineering Education in 1997, the Award for Persons of scientific and technological merits (Commendation by the minister of state for Science and Technology), the IEE Mountbatten Premium Award in 1999 and the Best Paper Award at the 1999 IEEE International Symposium on Intelligent Signal Processing and Communication Systems. He also received the IEEE Third Millennium Medal in 2000. He received the fellow grade from IEEE and SICE.

Hiroshi Inokawa received B.S., M.S., and Ph.D. degrees in electrical engineering from Kyoto University in 1980, 1982 and 1985, respectively. In 1985, he joined Atsugi Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation (NTT), Kanagawa, Japan. Since then, he has been engaged in the research and development of scaled-down MOS devices including those with reduced parasitic effects, and advance isolation schemes. His current work includes research on silicon nanodevices, particularly single-electron devices, and their applications. He is now a Senior Research Engineer, Supervisor at NTT Basic Research Laboratories. Dr. Inokawa is a member of the Japan Society of Applied Physics, and IEEE.

Yasuo Takahashi received B.S., M.S., and Ph.D. degrees in electronics in 1977, 1979, and 1982, respectively, from Tohoku University, Sendai, Japan. Since joining NTT in 1982, he has been engaged in research on the physics and chemistry of semiconductor surfaces and interfaces. His work includes research on the quantum physics of Si nanostructures and their electronic device applications. Since 2004, he has been a professor at the Graduate School of Information Science and Technology, Hokkaido University, Sapporo, Japan. Dr. Takahashi is a member of the Japan Society of Applied Physics, the Institute of Electrical Engineers of Japan, and IEEE.